9TH LETI MEMORY WORKSHOP

Grenoble June 27th

AN INSIGHT INTO THE HIGH TEMPERATURE RELIABILITY OF N-DOPED AND Ge-RICH GeSbTe PHASE CHANGE MEMORIES

V. Sousa[1], G. Navarro[1], N. Castellani[1], J. Kluge[1, 2], O. Cueto[1], C. Sabbione[1], A. Roule[1], V. Delaye[1], N. Bernier[1], F. Fillot[1], P. Noé[1], L. Perniola[1], S. Blonkowski[2], M. Borghi[2], E. Palumbo[2], P. Zuliani[2], R. Annunziata[2]

[1] CEA-LETI-MINATEC Campus
[2] STMicroelectronics

OUTLINE

1. Background and Objectives
2. Thin Film Characterization
3. Device Characterization
4. Analysis of the Programmed States
   - Morphological Characterization
   - Simulation of the Programming Operations
5. Conclusions

OUTLINE

1 **Background and Objectives**

2 Thin Film Characterization

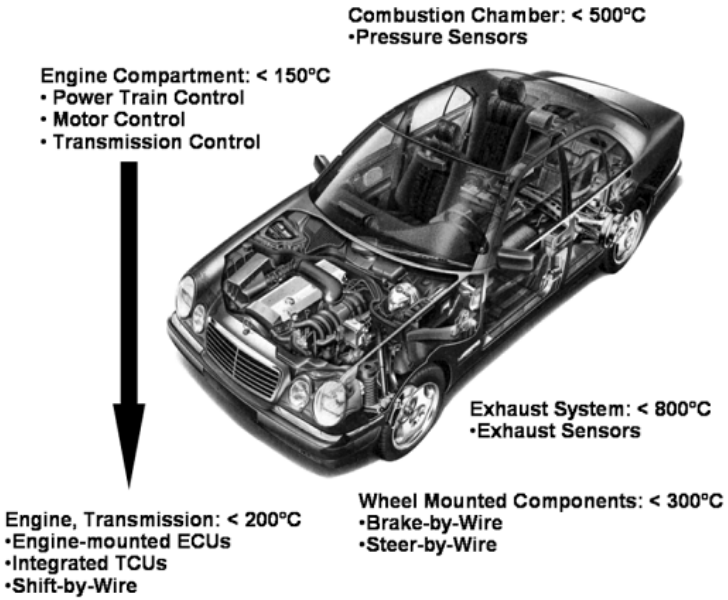
3 Device Characterization

4 Analysis of the Programmed States
- Morphological Characterization
- Simulation of the Programming Operations

5 Conclusions

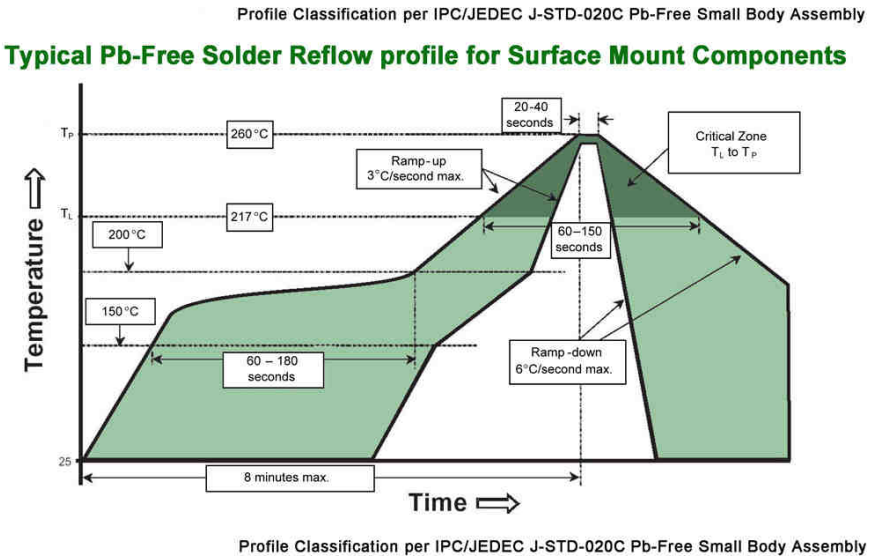
WHY A HIGH THERMAL STABILITY FOR eNVM ?

- **Automotive applications challenge electronics at above 125 °C.**

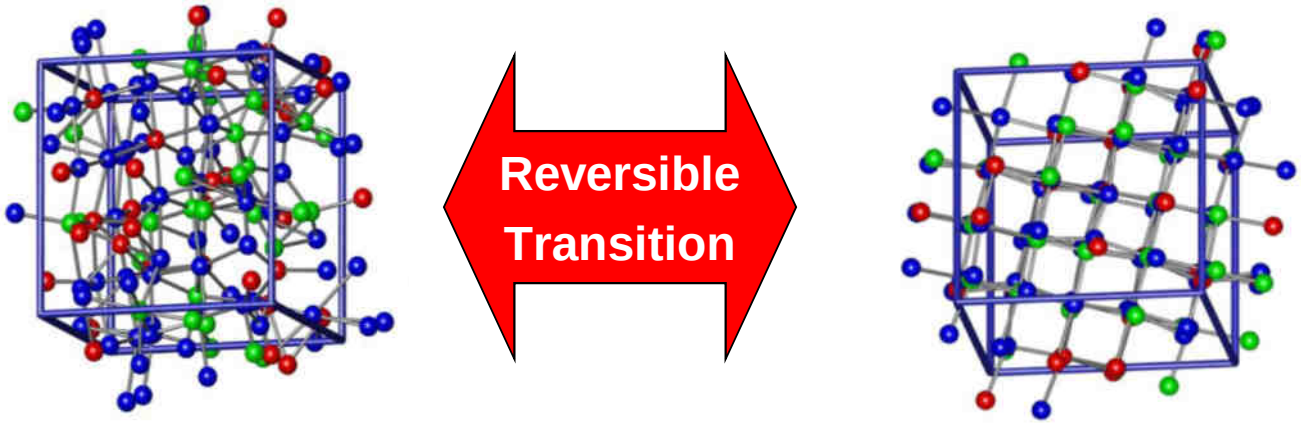


R. Wayne Johnson et al. TEPM (2004)

- **Solder Reflow temperature profile → peak @ 260°C**

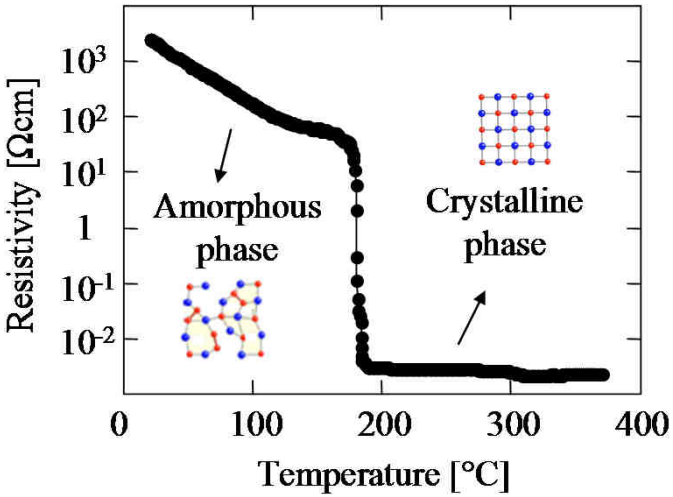


PHASE-CHANGE MATERIALS

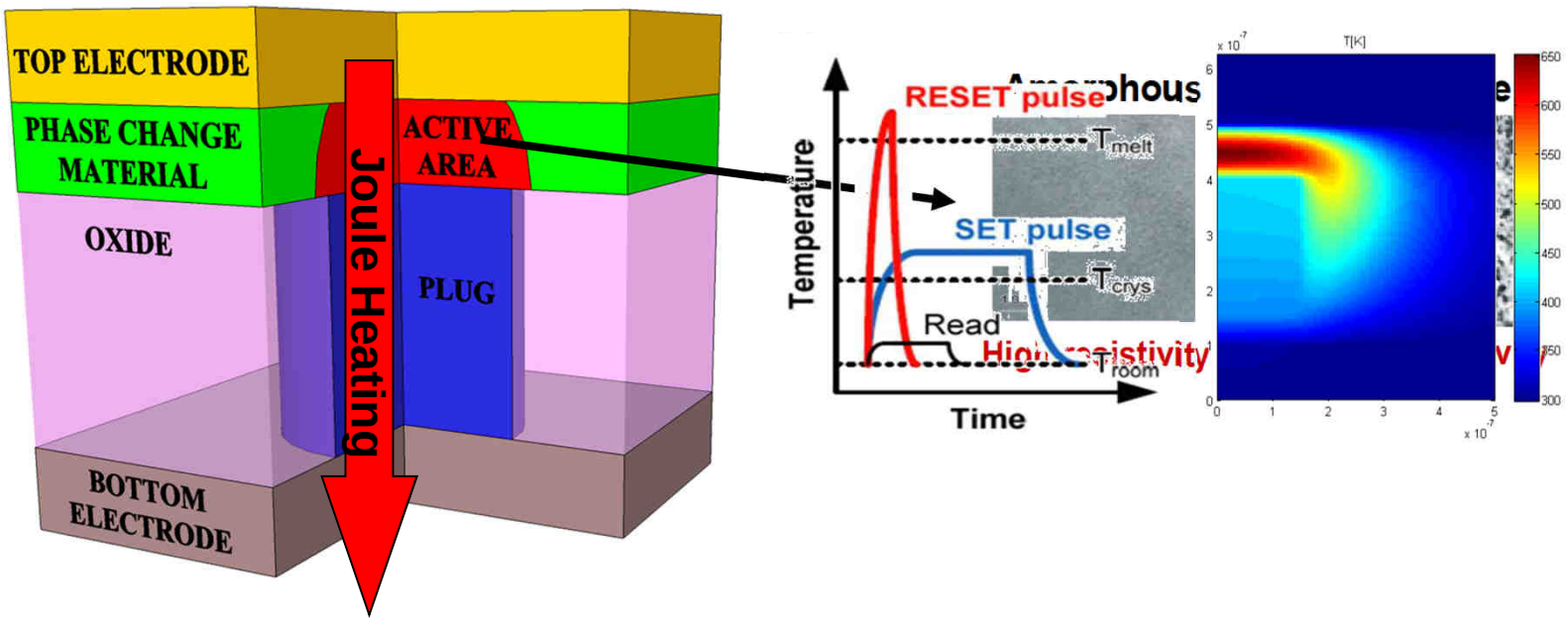


AMORPHOUS PHASE **CRYSTALLINE PHASE**

- **Chalcogenide materials are alloys based on VI group elements**
- **Exhibit reversible transition (Phase-Change) e.g. $Ge_2Sb_2Te_5$ (GST) or GeTe**
- **High contrast between resistivity of amorphous and crystalline phase**



THE PCM CELL CONCEPT



- **Information stored in the resistance of the chalcogenide alloy (Crystalline / Amorphous).**
- **Phase transition of chalcogenide alloy obtained by current-induced Joule heating.**

PCM PERFORMANCE VS MATERIAL PROPERTIES

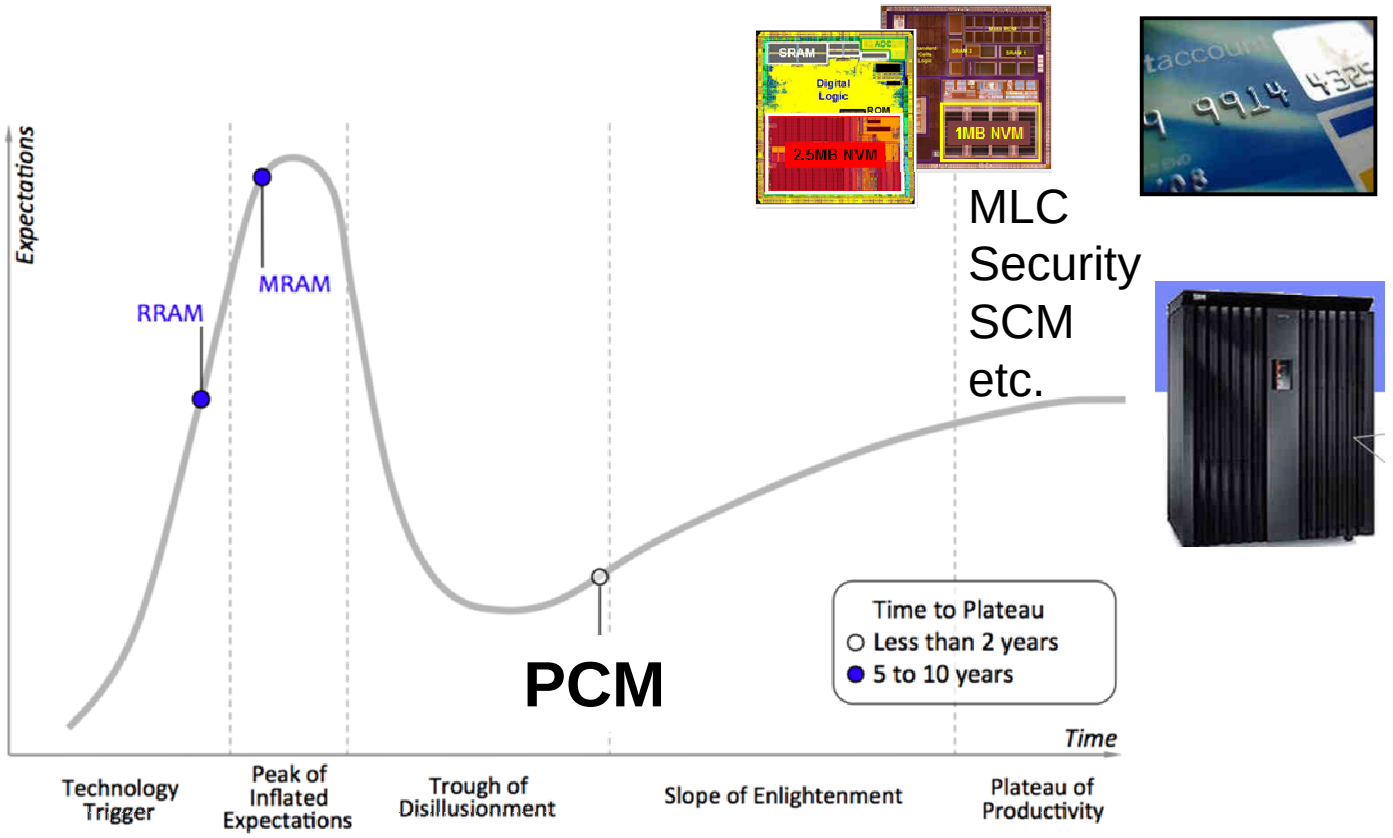
PERFORMANCE	MATERIAL PROPERTIES
Speed	Crystallization Speed
Programming Power	Material thermal & electrical conductivity, geometry
Data Retention	Amorphous phase thermal stability
Endurance & Life Time	Material composition stability

PCM TODAY

Phase-Change Memory 

- Non-volatile memory technology
- Compatible with CMOS Back-End-Of-Line
- Fast access time (~10ns)
- Fast write/erase (~100ns)
- Low voltage operation (< 3V)
- Large Roff/Ron (~1000)
- High endurance (up to 10^{12})
- Good scalability

PCM HYPE CYCLE



C.H. Lam, IEDM 2014

Phase-Change Memory: a flexible technology for a memory market in constant diversification.

PCM TODAY

Phase-Change Memory 

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PCM CHALLENGES

Phase-Change Memory

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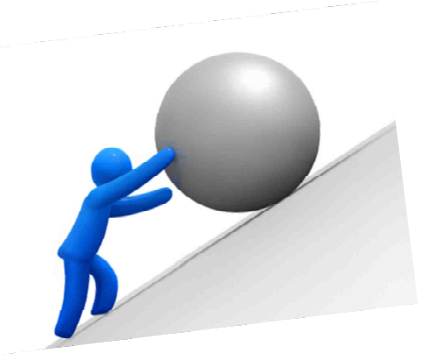
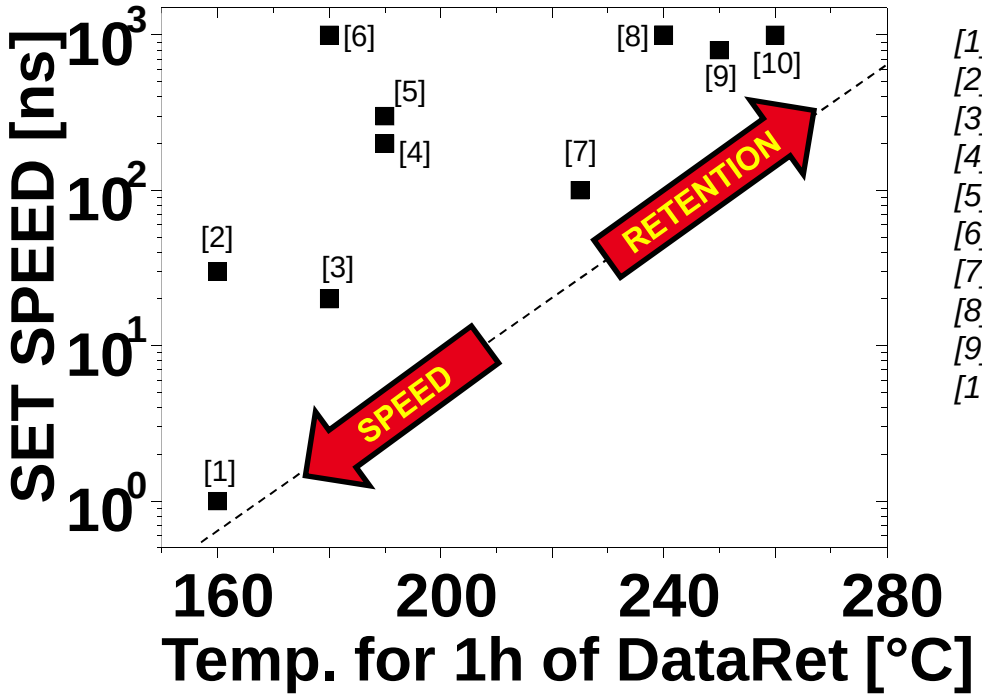


CHALLENGES

✓ Improve the Thermal Stabilty of the programmed states

PCM SPEED VS RETENTION: A MATTER OF COMPROMISE

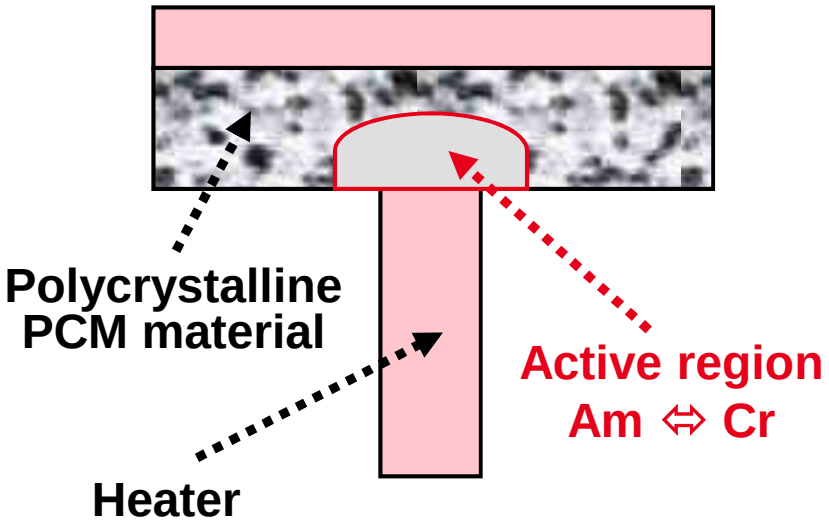


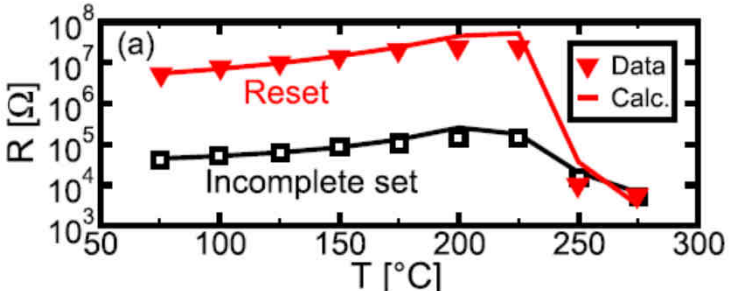
[1] Cheng Peng et al., J. Appl. Phys. 2013
[2] F. Pellizzer et al., VLSI 2004
[3] G. Navarro et al., IRPS 2013
[4] H. Y. Cheng et al., IEDM 2011
[5] H. Y. Cheng er al., IEDM 2012
[6] G.B. Beneventi et al., IMW 2010
[7] A. Fantini et al., IEDM 2010
[8] P. Zuliani et al., TED 2013
[9] S.H. Lee et al., IEDM 2011
[10] G. Navarro et al., IEDM 2013

- Phase-Change Material Engineering can boost PCM performance
- Trade-off to be found between SET Speed and Data Retention

THERMAL STABILITY ISSUES WITH PCM DEVICES

- **The thermal stability of the programmed states can be compromised by:**
  - The crystallization ⇨ Resistance decay ↘ ⇨ RESET failure





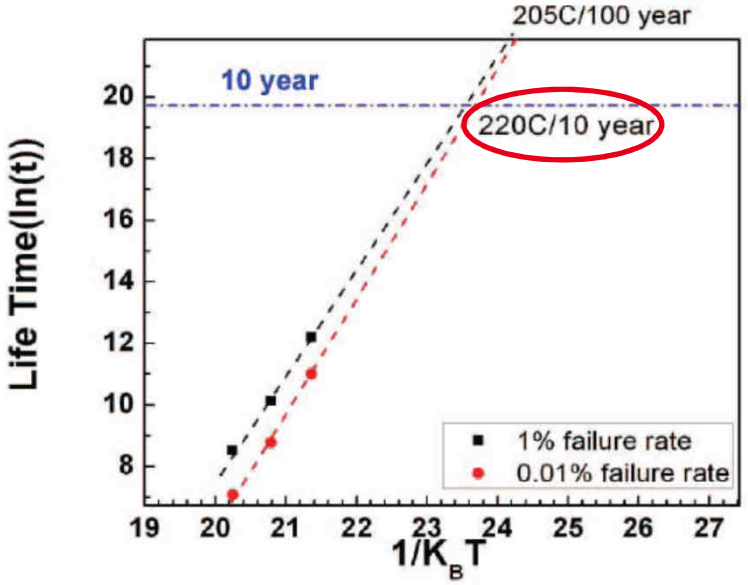
Ciocchini et al. TED (2014)

PCM MATERIALS WITH HIGH TEMPERATURE RELIABILITY

- **GaSb-Ge materials (10ys @ 220 °C)**
  validated in a 128Mbit test vehicle

  Pass the soldering criteria ☑

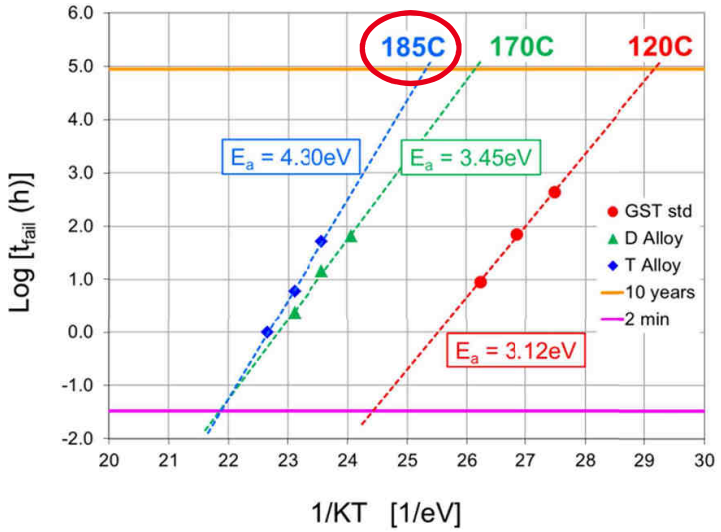
  H. Y. Cheng et al., IEDM 2015.



- **Ge-rich GST materials (10ys @ 185 °C)**
  validated in a 12Mbit test vehicle.

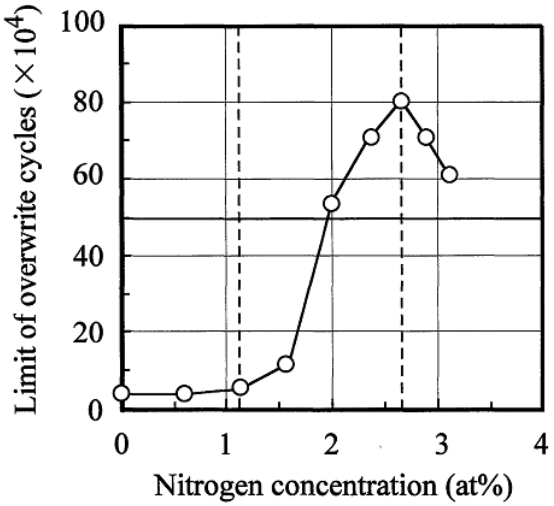
  Pass the soldering criteria ☑

  P. Zuliani et al., IEEE Trans. Electron Devices, 2013.



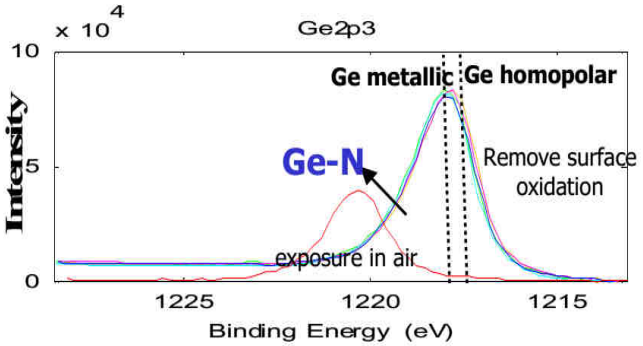
N-DOPING IN PCM COMPOUNDS

- **N doping in Ge-Sb-Te recording layer (Optical Disks) improves their recording sensitivity, erasability and overwrite cycles.**



Rie Kojima et al.,
Jpn. J. Appl. Phys. 37 2098 (1998).

- **N doping in GexSbyTez compounds suppresses the elemental segregation indicating a better endurance performance.**



H. Y. Cheng et al., IEDM 2012.

Ge-RICH GST MATERIALS FOR ePCM

- **High reliability performances of Ge-rich GST devices**
  - High thermal stability of the RESET state wrt crystallization
  - Low drift of the SET state wrt structural relaxation

OBJECTIVES OF THE STUDY

- **Highlight the benefits of N-doping in Ge-rich GST**
- **Provide an insight into the operation fundamentals of N-doped and Ge-rich GST storage elements**

OUTLINE

1 Background and Objectives

2 **Thin Film Characterization**

3 Device Characterization

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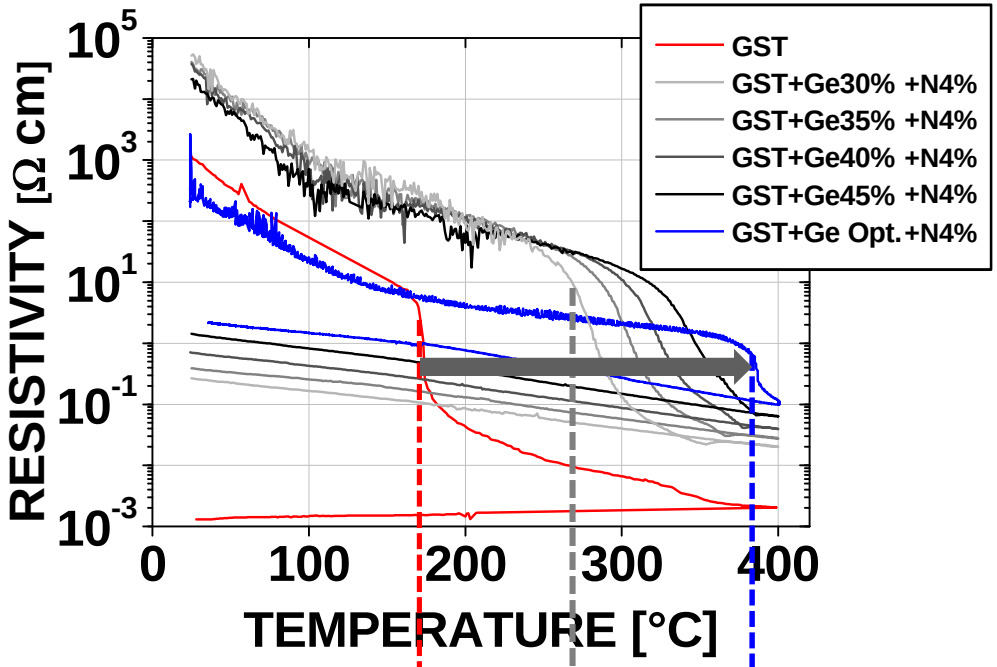
5 Conclusions

THIN FILM CHARACTERIZATION

ELECTRICAL RESISTIVITY VERSUS T
→ CRYSTALLIZATION TEMPERATURE Tc



« GST + Ge x% + N4% »

Co-sputtering
from $Ge_2Sb_2Te_5$ + Ge

GST
T_c~170°C

GST+Ge30%+N4%
T_c~260°C

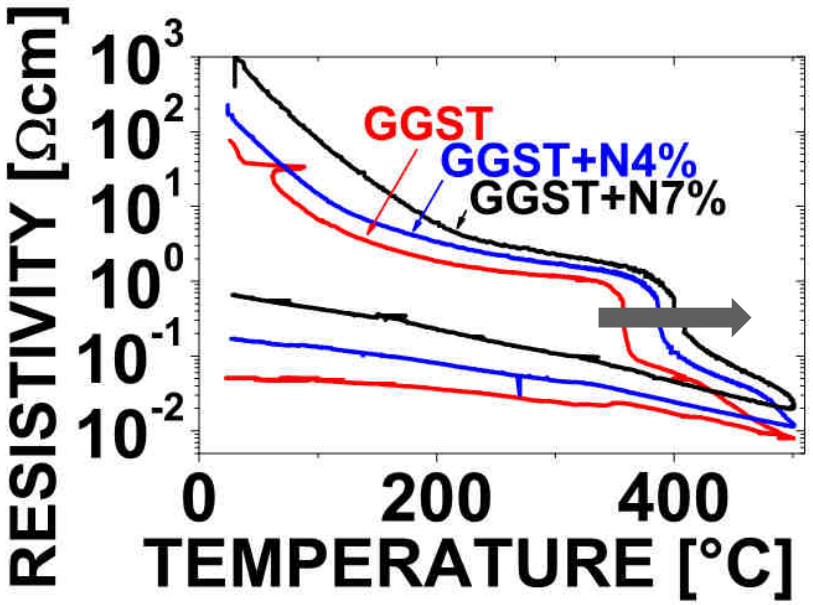
GST+Ge opt.+N4%
T_c~380°C

Increase of Ge at. % → Increase of T_c

THIN FILM CHARACTERIZATION

ELECTRICAL RESISTIVITY VERSUS T
→ CRYSTALLIZATION TEMPERATURE Tc

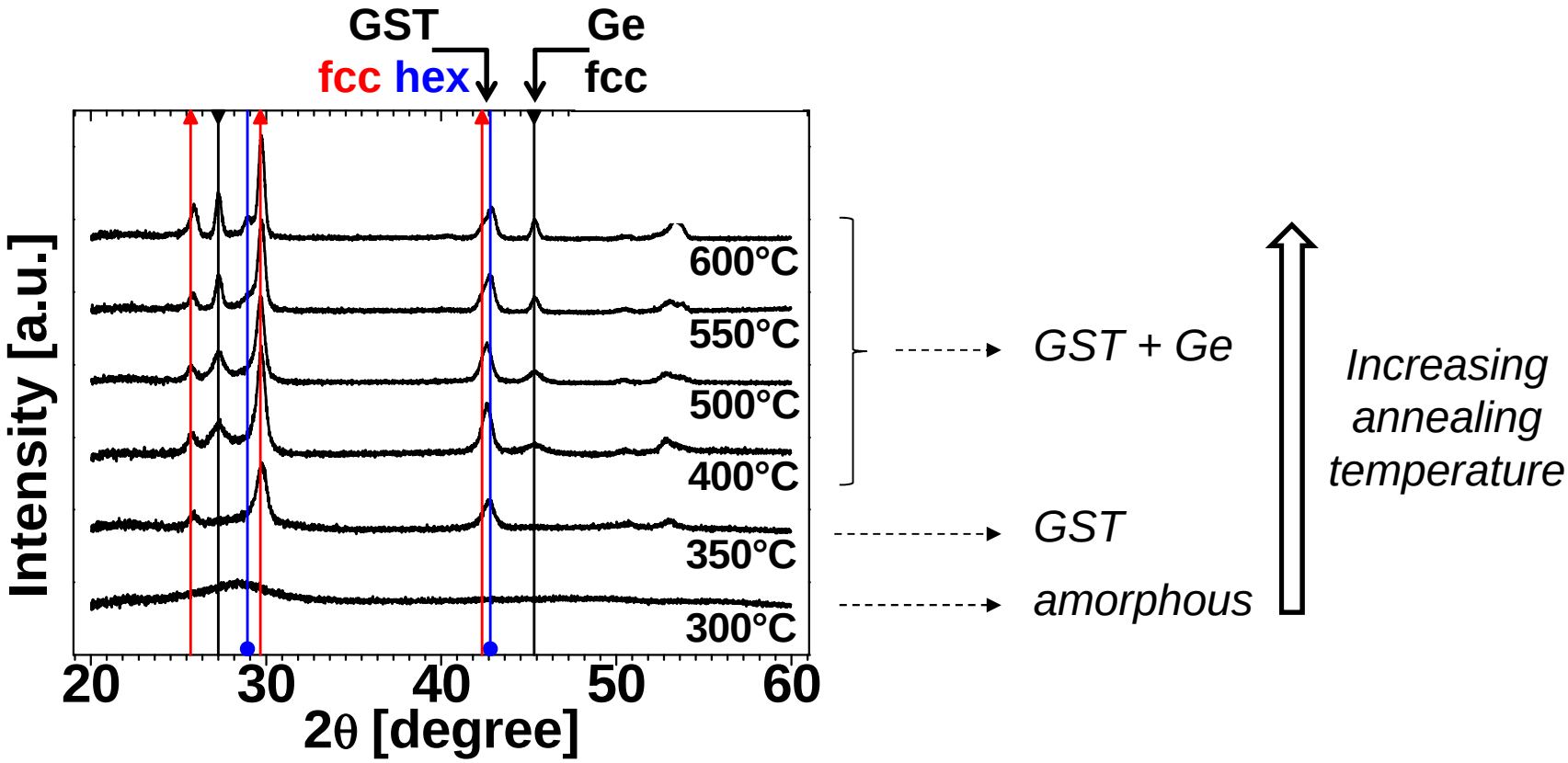
Effect of N additions in GST+Ge opt.



N-doping in Ge-rich GST → Increase of T_c

THIN FILM CHARACTERIZATION

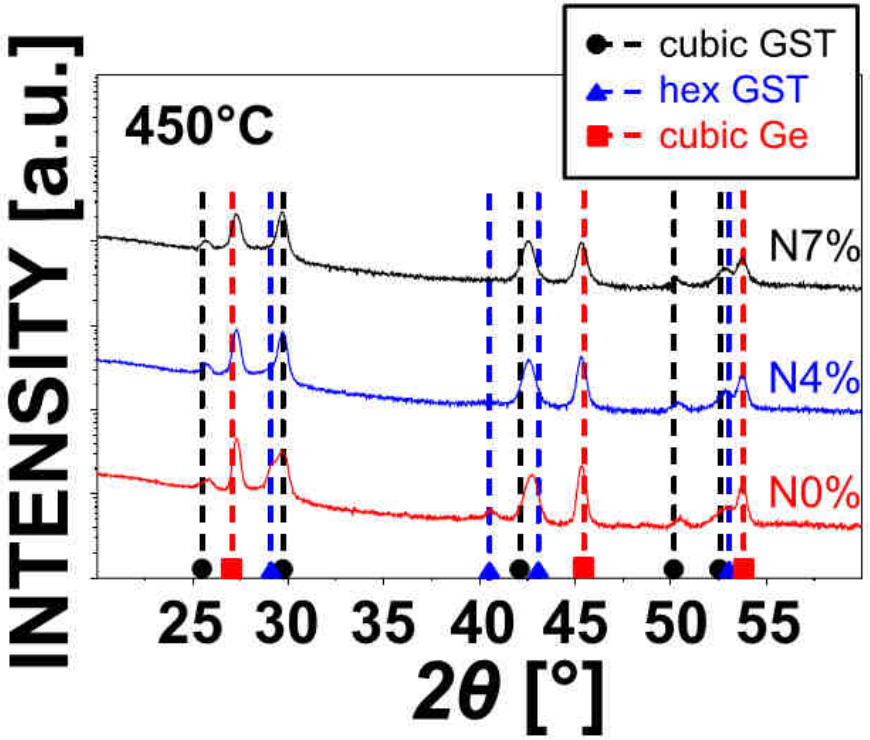
X-RAY DIFFRACTION → CRYSTALLINE STRUCTURE



Ge-rich GST crystallization → Phase separation GST + Ge.

THIN FILM CHARACTERIZATION

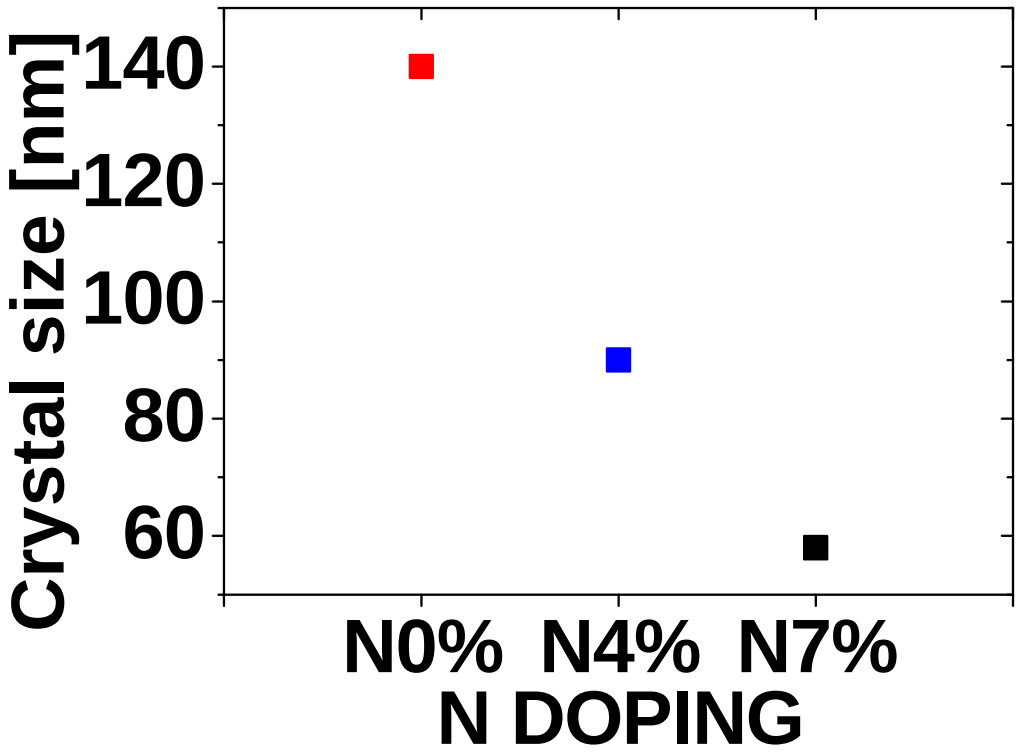
X-RAY DIFFRACTION → CRYSTALLINE STRUCTURE



Ge-rich GST, w/o or with N-doping → Phase separation GST + Ge

THIN FILM CHARACTERIZATION

X-RAY DIFFRACTION → GRAIN SIZE

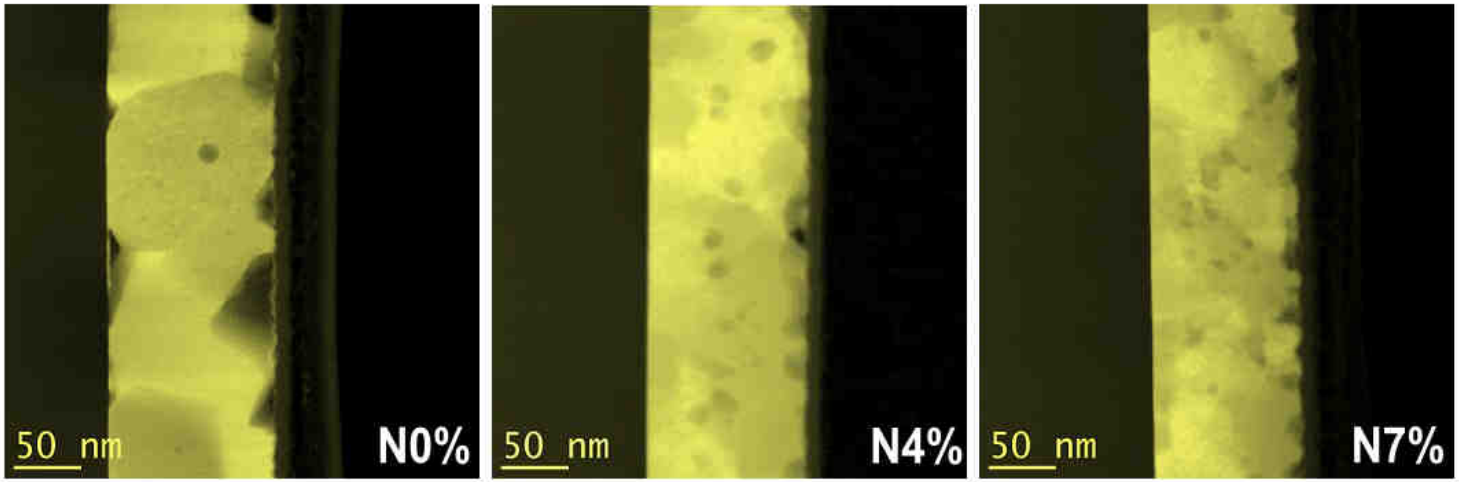


Ge-rich GST, with increasing N-doping → Smaller grain size

THIN FILM CHARACTERIZATION

HAADF/STEM IMAGING

450 °C annealing

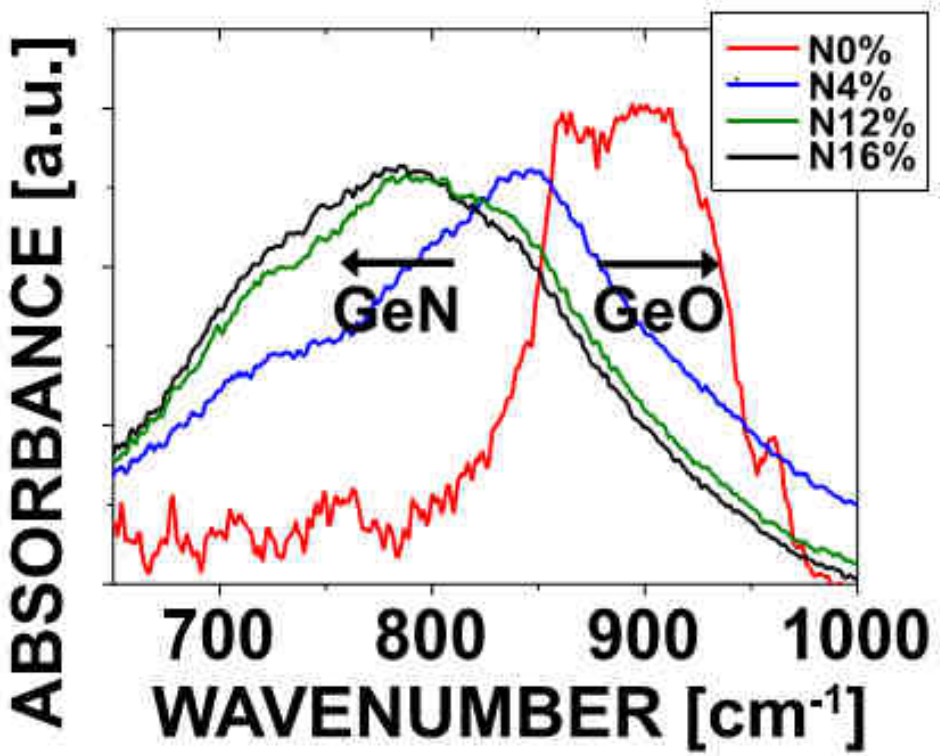


w/o N doping
↓
Large grain size
↓
Local density lowering

with N-doping
↓
Small grain size

THIN FILM CHARACTERIZATION

FTIR ANALYSIS



Ge-rich GST with N-doping → Lower Ge-O peak intensity

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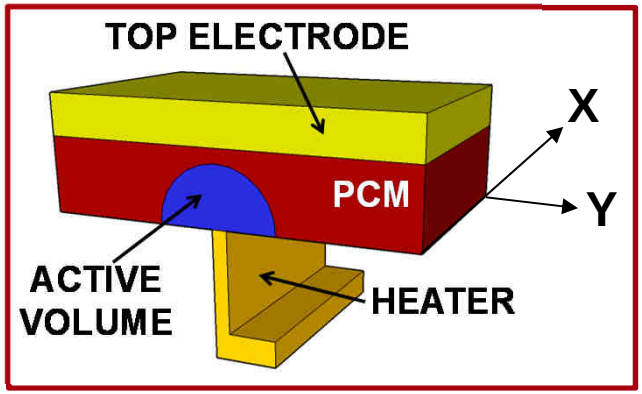
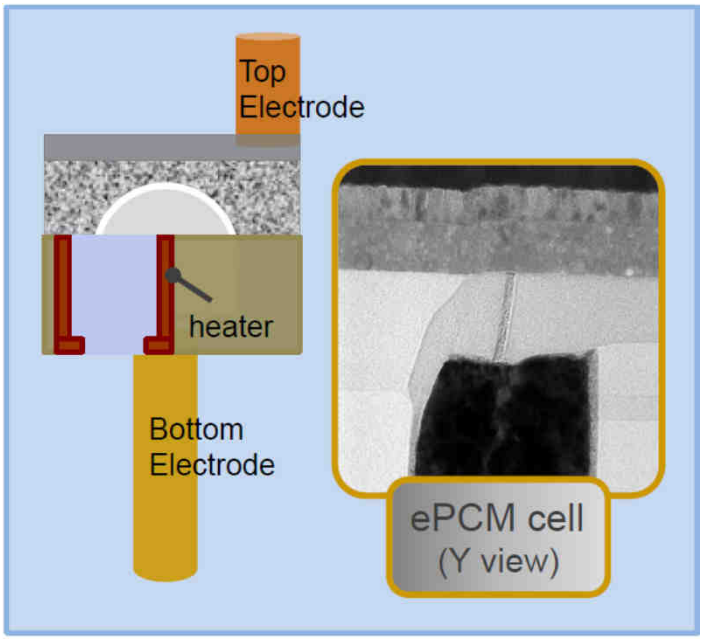
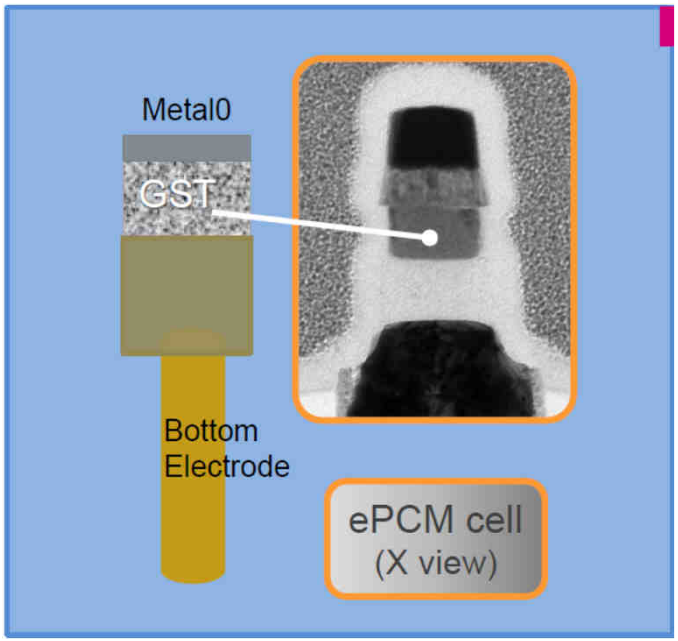
DEVICE PRESENTATION



Wall storage element
Aggressive 90nm technology node

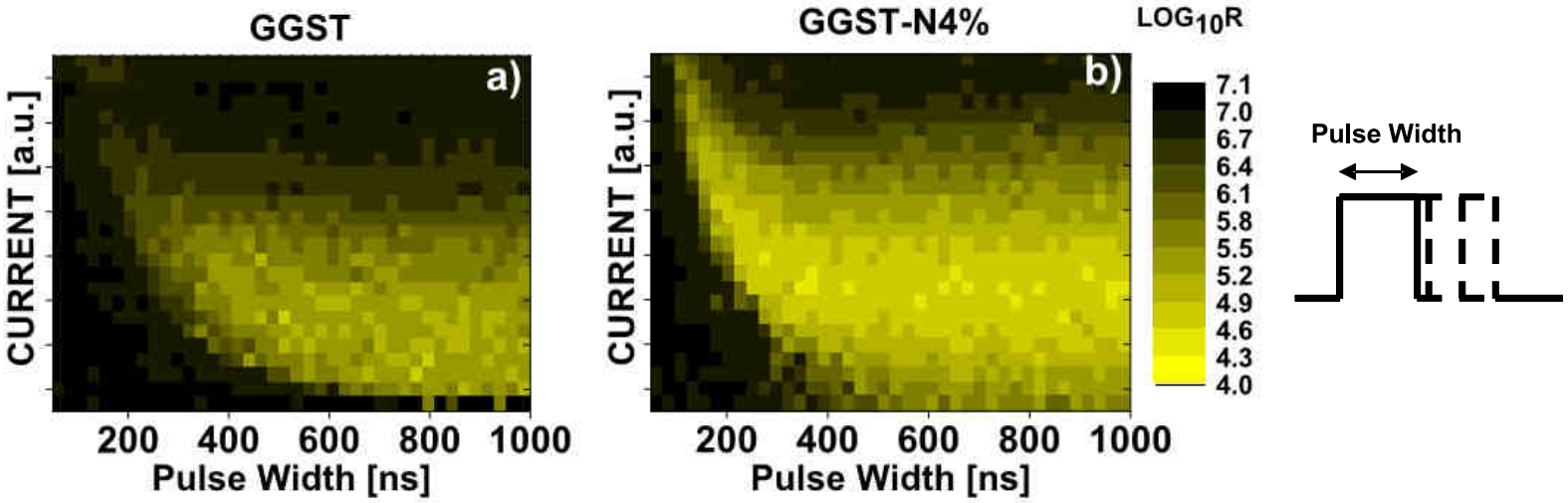




Source: P. Zuliani, presented at the « eNVM workshop » Gardanne, Sept 2013

DEVICE CHARACTERIZATION

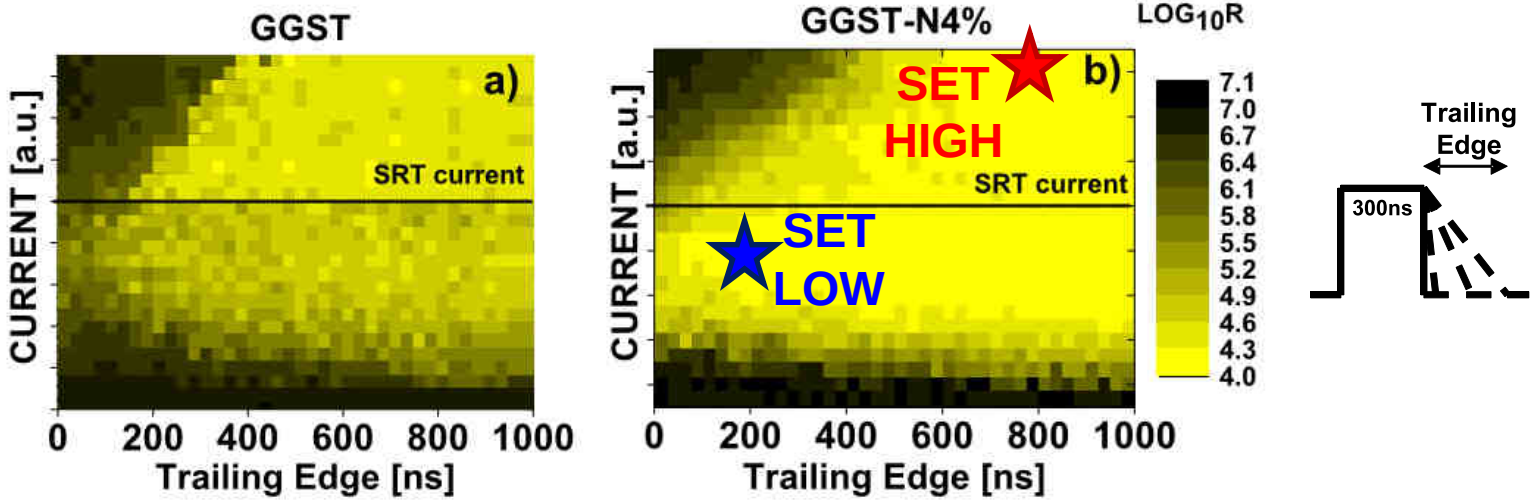
CRYSTALLIZATION CARTOGRAPHIES
SET SPEED ANALYSIS



Ge-rich GST with N-doping → A lower resistance state is achievable

DEVICE CHARACTERIZATION

CRYSTALLIZATION CARTOGRAPHIES
SET SPEED ANALYSIS

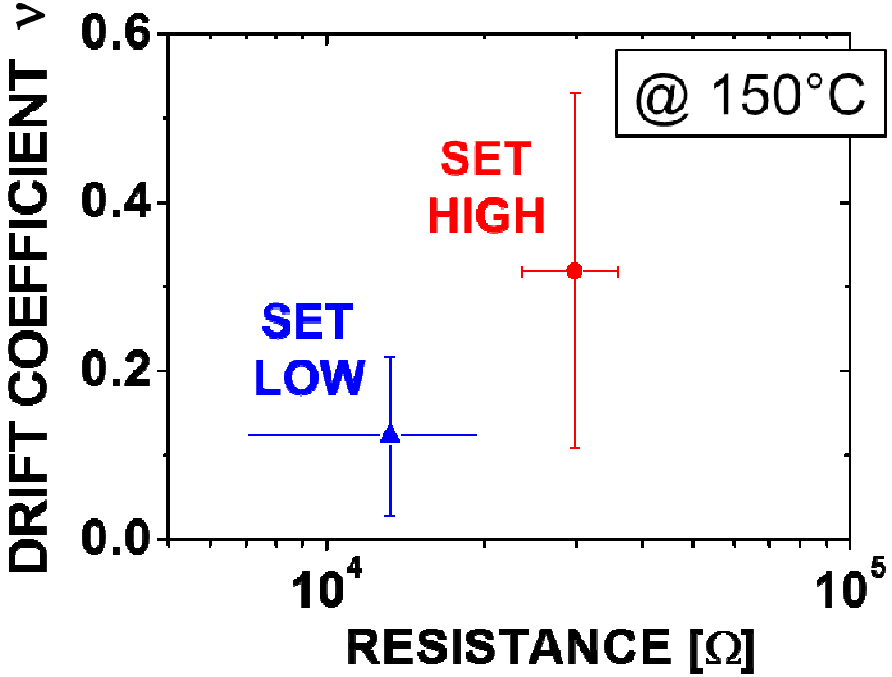


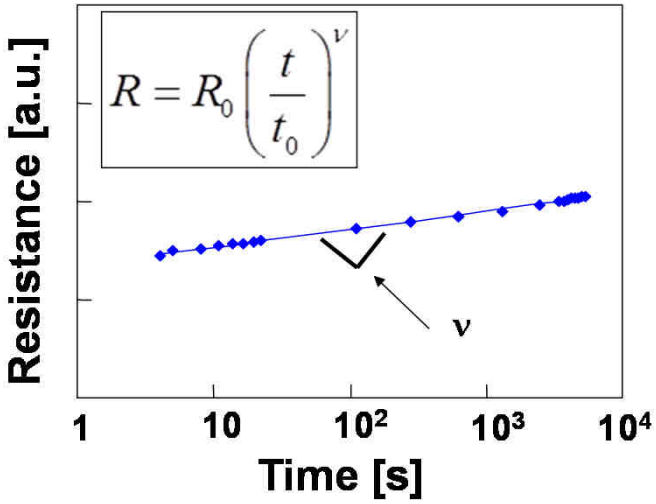
Ge-rich GST with N-doping → SET programming is more efficient

Two different programming conditions for SET:
SET_low & SET_high

DEVICE CHARACTERIZATION

SET STATE DRIFT

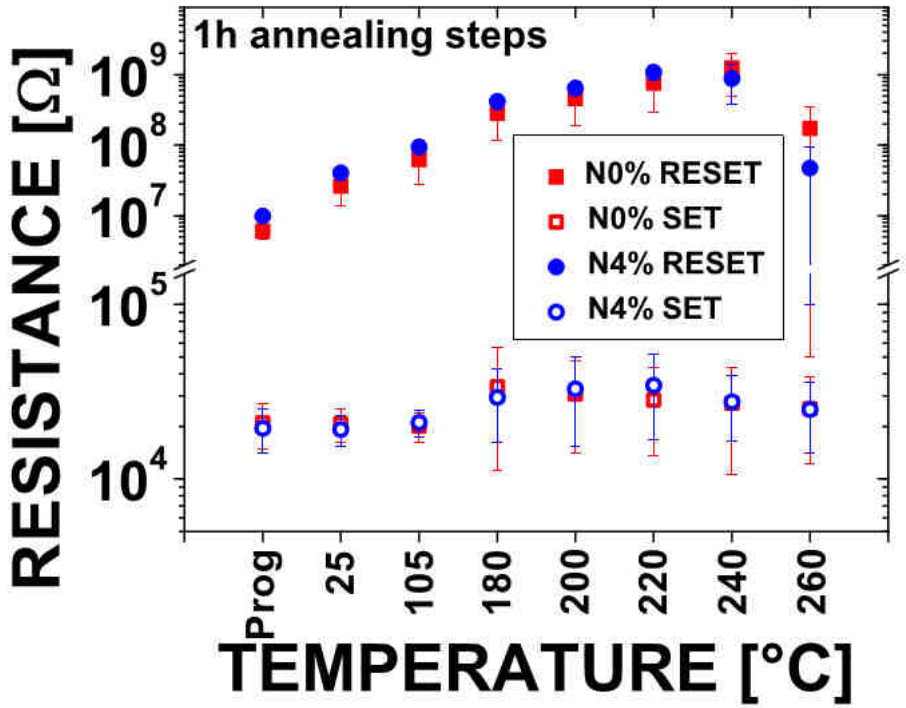




SET at LOW current → low resistance & low drift

DEVICE CHARACTERIZATION

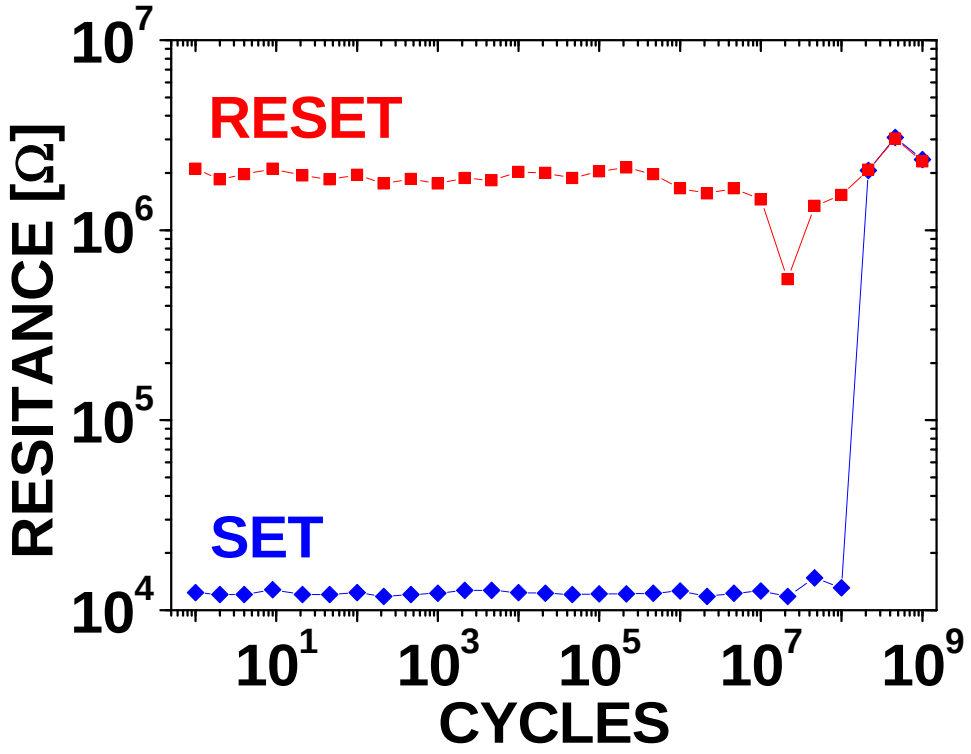
THERMAL STABILITY OF THE PROGRAMMED STATES



Ge-rich GST, w/o or with N-doping
→ RESET state retention is granted up to 240 °C.

DEVICE CHARACTERIZATION

ENDURANCE

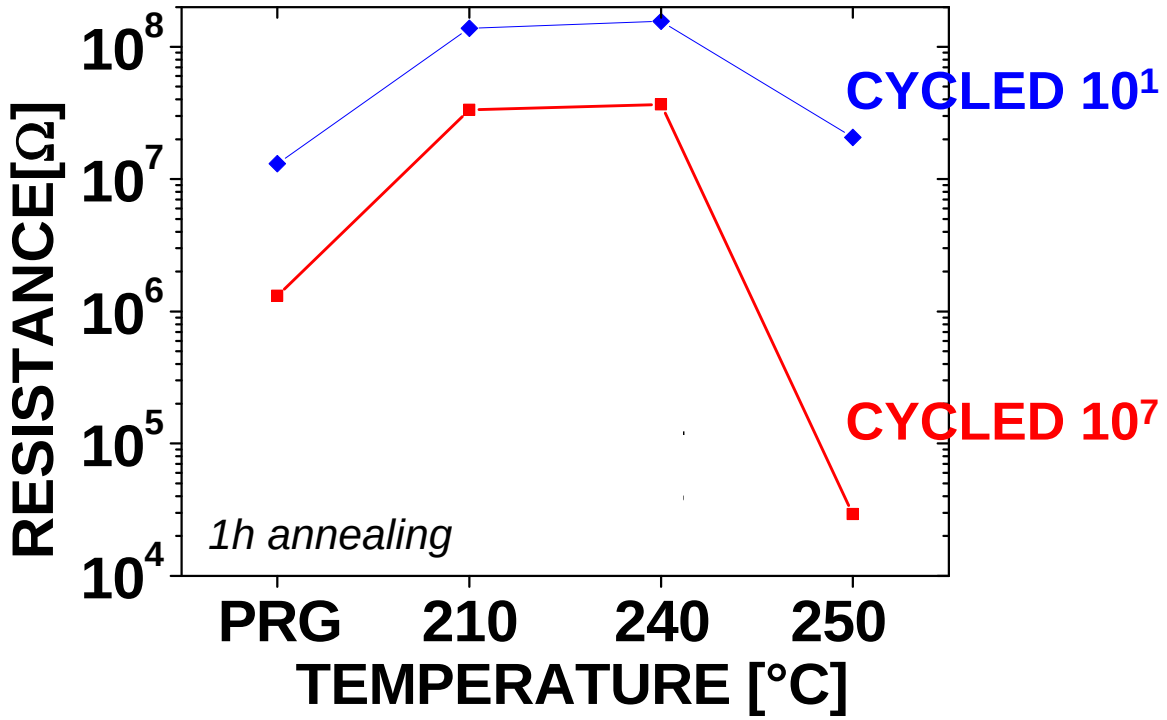


RESET: 30ns 400µA
SET: 800ns 200µA

Stability of the reading window up to at least 10^7 cycles.

DEVICE CHARACTERIZATION

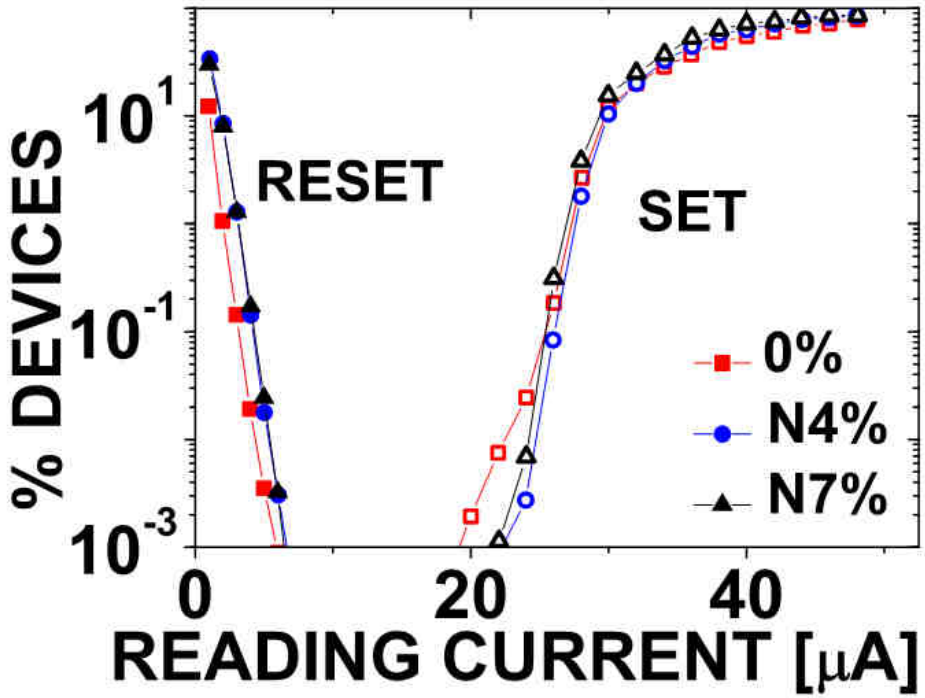
THERMAL STABILITY AFTER CYCLING



After 10^7 SET/RESET cycles,
the fail temperature is lowered by only 10°C at maximum.

12Mb TEST VEHICLE CHARACTERIZATION

SET/RESET RESISTANCE DISTRIBUTIONS



Ge-rich GST, w/o or with N-doping → Reliable reading window for the intrinsic parts of the distributions (> 0.001%).

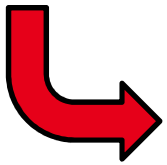
N-DOPED AND Ge-RICH GST DEVICE PERFORMANCES

SUMMARY

- Optimized SET operation <u>at low current</u>

  → low resistance & low drift

- Stability of the SET & RESET states for <u>1h at 240°C</u>



MORPHOLOGICAL CHARACTERIZATION OF THE PROGRAMMED STATES

Representative alloy: GST+Ge45%+N4%

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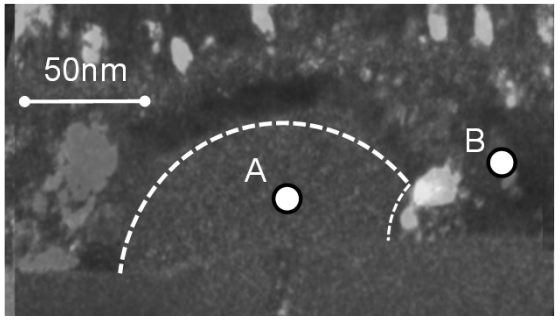
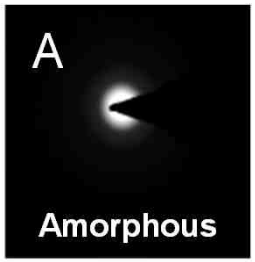
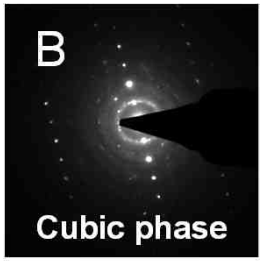
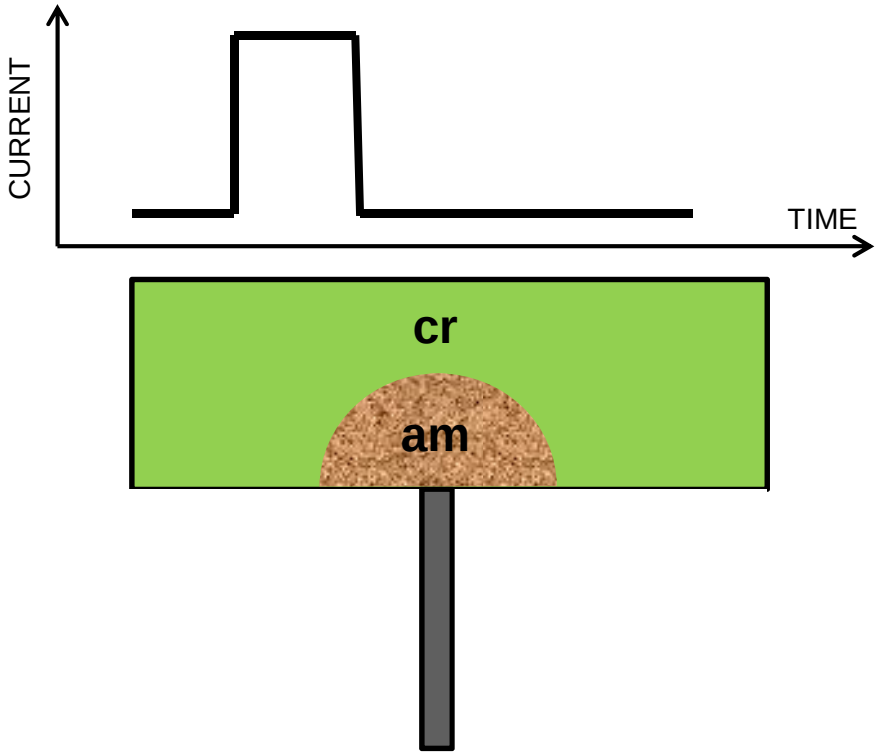
DEVICE CHARACTERIZATION

THE RESET STATE





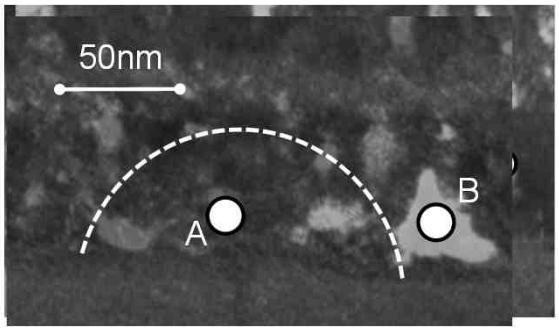


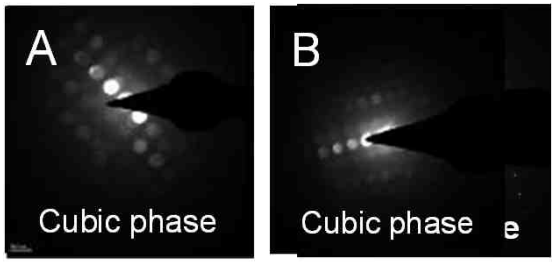


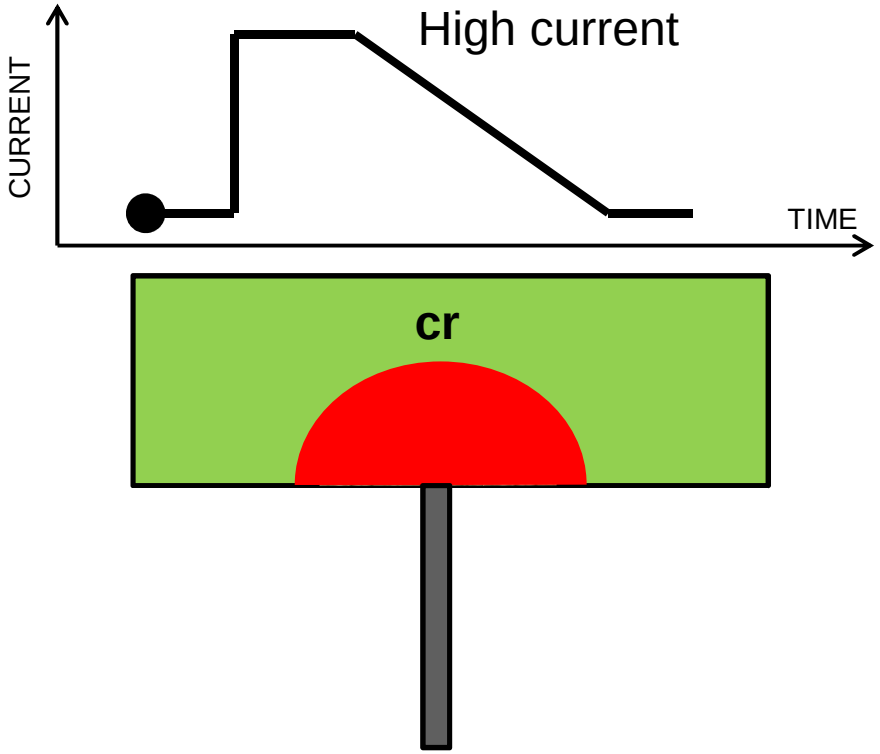
- Amorphous dome within a polycrystalline PCM layer.

DEVICE CHARACTERIZATION

THE SET_HIGH STATE





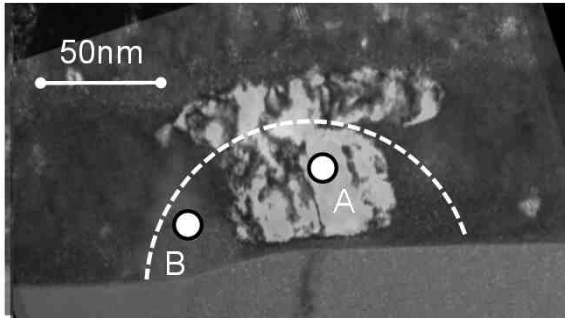


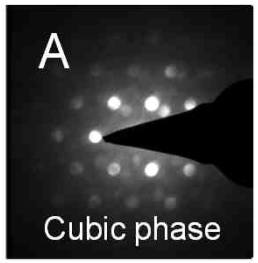
- Fully polycrystalline PCM layer with randomly oriented grains.
- High number of GBs → high SET state drift*.

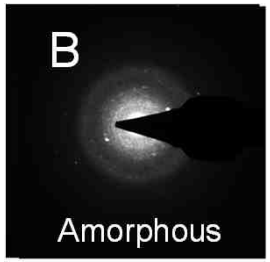
* *N. Ciocchini et al., TED 2014.*

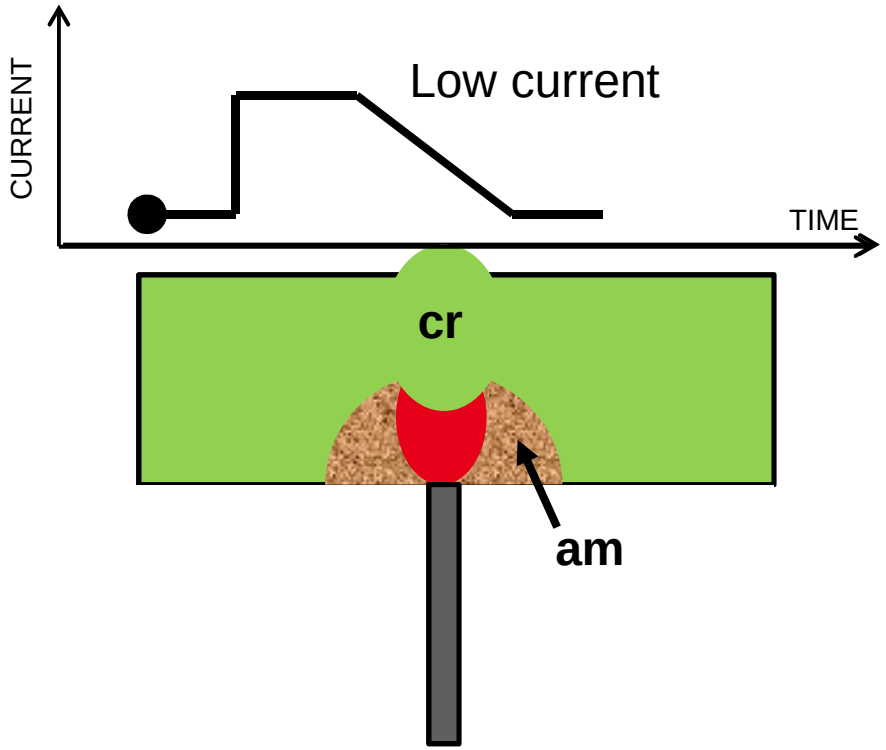
DEVICE CHARACTERIZATION

THE SET_LOW STATE



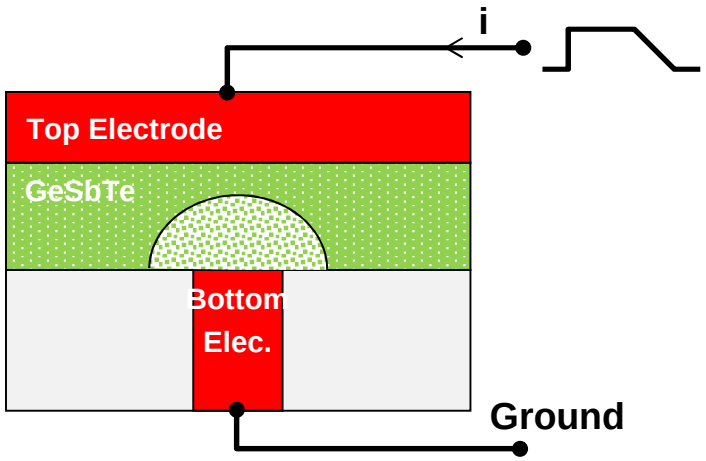






- Partially crystalline PCM layer.
- Single crystalline orientation along the conductive path.
- Low number of GBs → Lower drift wrt SET HIGH

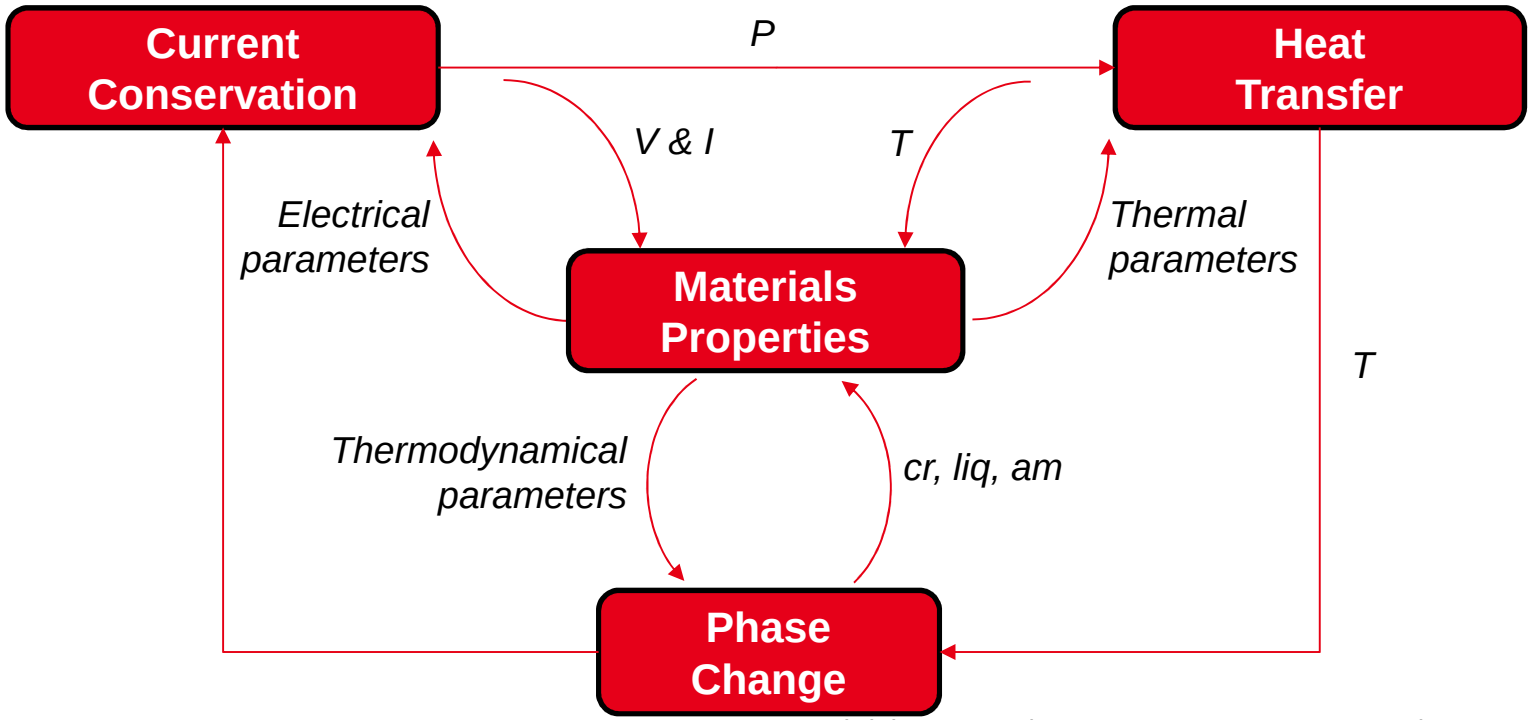
MULTIPHYSICAL SIMULATIONS



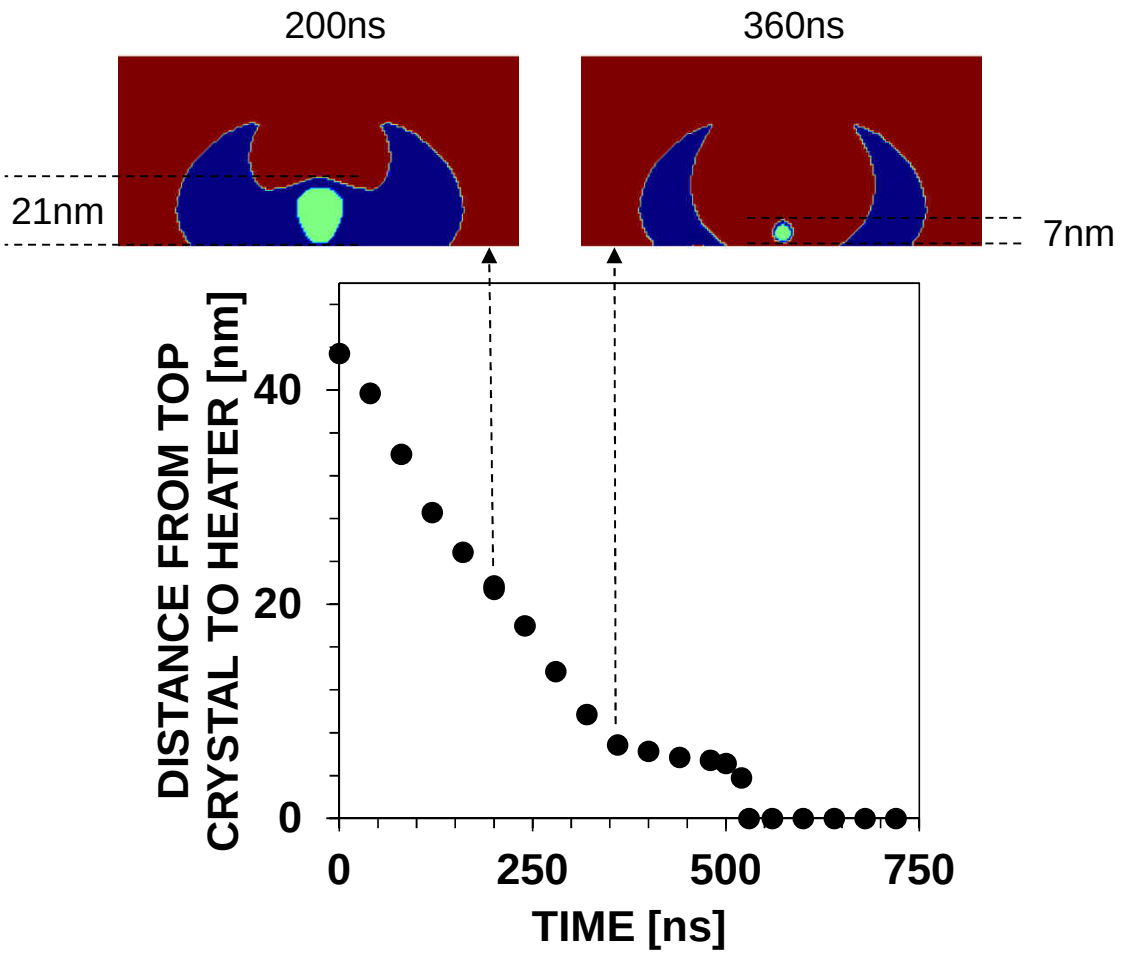
A. Glière et al., IEEE Conf. SISPAD (2011)

O. Cueto al., IEEE Conf. SISPAD (2012)

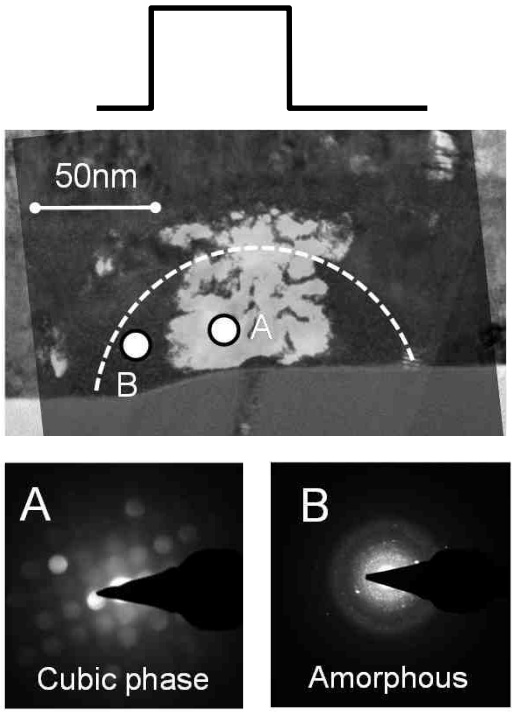
O. Cueto al., IEEE Conf. SISPAD (2015)



SIMULATION: THE SET_LOW OPERATION



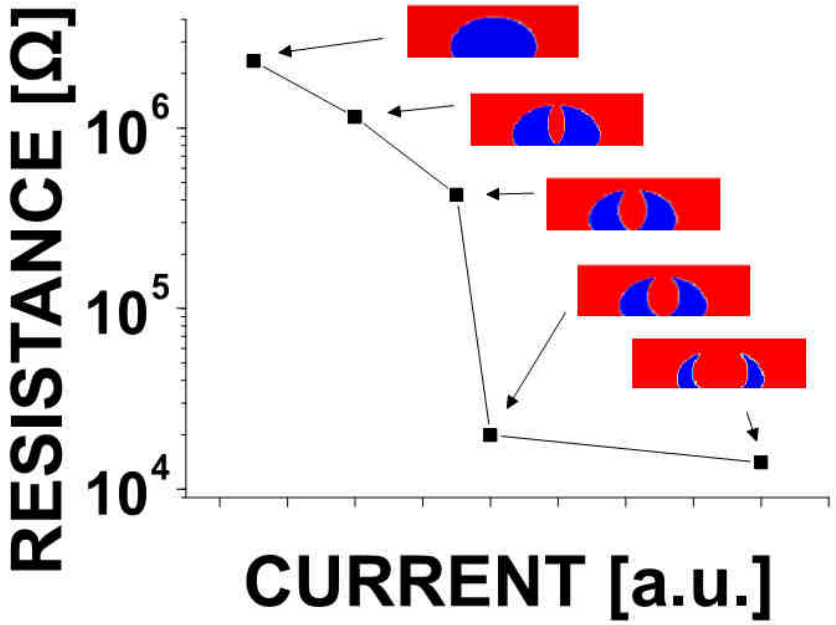
SET_LOW
w/o trailing edge



Good agreement between simulations, electrical results & TEM

ELECTROTHERMAL SIMULATIONS

PROGRAMMING CHARACTERISTICS R(I)



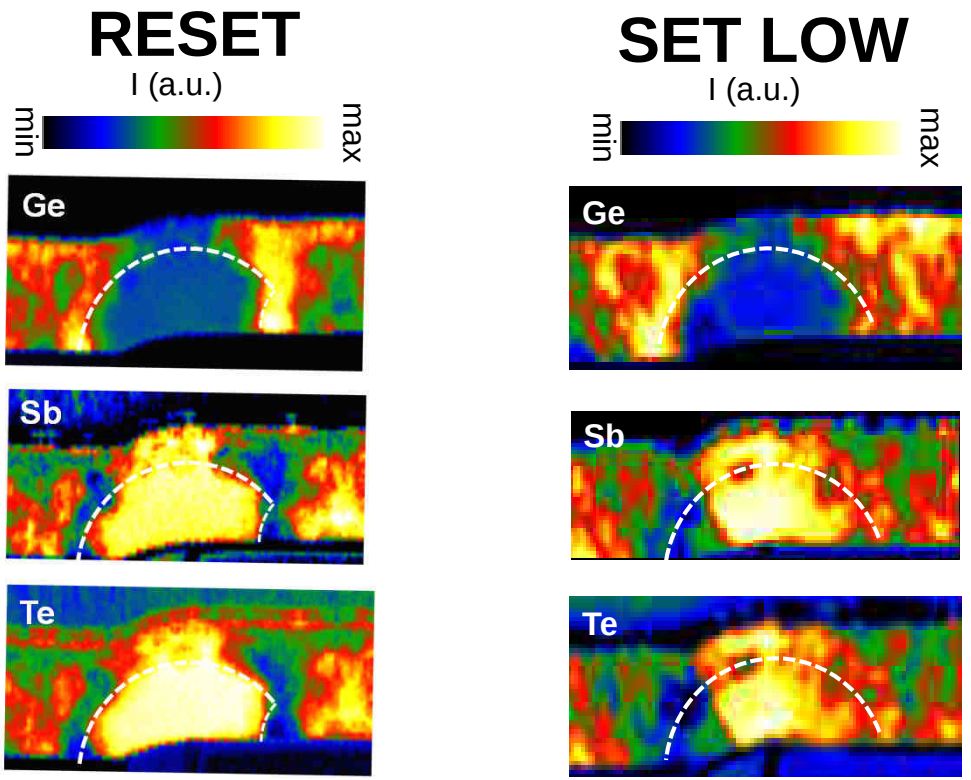
- Demonstration of the SET operation at performed at low current
- N-doping → No large Ge grains that can cross the conductive path made of GST grains → Reliable SET operation.

DEVICE CHARACTERIZATION

STEM/EELS ANALYSIS → ELEMENTAL DISTRIBUTION

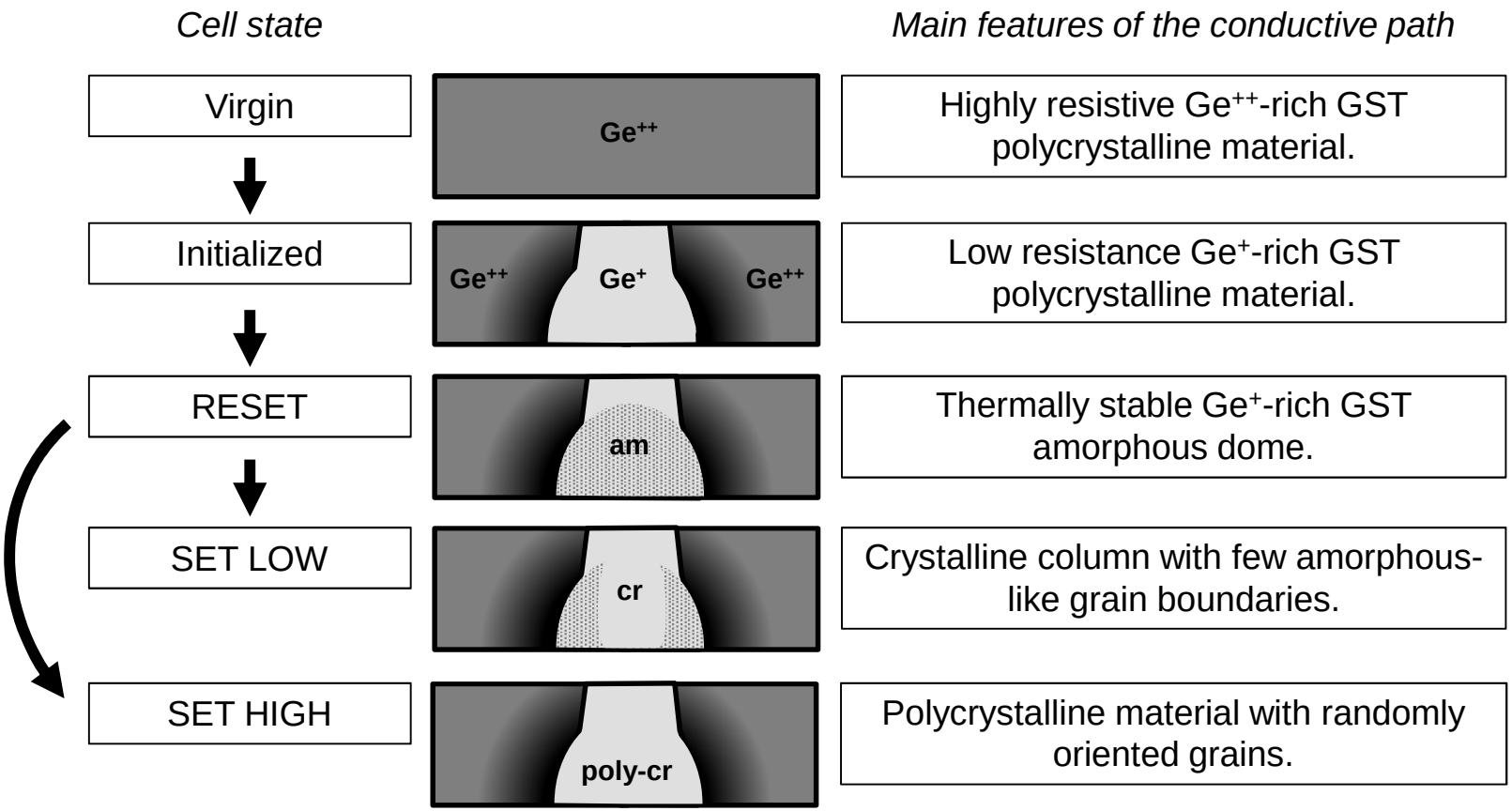
Core composition
~ GST+Ge25%

→ T_c ~ 250°C



- Ge-depletion from the heater up to the top electrode.
- Lateral Ge-rich zones are crystalline
- Segregation effect likely to result from the initial seasoning.

UNDERSTANDING THE HIGH THERMAL STABILITY OF N-DOPED AND Ge-RICH GST BASED PCM DEVICES



OUTLINE

1 Background and Objectives

2 Thin Film Characterization

3 Device Characterization

4 Analysis of the Programmed States
- Morphological Characterization
- Simulation of the Programming Operations

5 **Conclusions**

AN INSIGHT INTO THE HIGH THERMAL STABILITY OF N-DOPED AND Ge-RICH GeSbTe BASED PCM DEVICES

CONCLUSIONS

Ge segregation at the periphery of the active area
+
Very high initial Ge content

⇩

Ge-rich alloy wrt GST at the core of the cell

⇩

High stability of the RESET state wrt crystallization

Peculiar crystallization mechanism of the SET_LOW operation

⇩

Only few amorphous-like grain boundaries along the conduction path

⇩

Low drift of the SET_LOW state

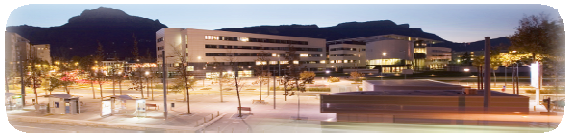
AN INSIGHT INTO THE HIGH THERMAL STABILITY OF N-DOPED AND Ge-RICH GeSbTe BASED PCM DEVICES

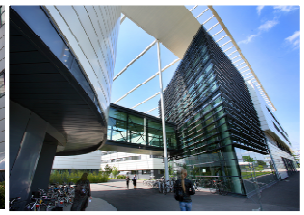
CONCLUSIONS

- N-doping can guarantee a **finer crystallization** structure of the phase-change material layer after BEOL.
- **SET operation reliability** is granted in N-doped GGST devices at low current, enabling faster and energy saving programming.
- Integration of Ge-rich and N-doped GST PCM materials was validated in a **12Mbit test vehicle**.
- The **good thermal stability** of N-GGST devices was proved by HTDR of 1 hour till 240 °C.
- **We confirm the PCM potential for embedded applications**.

9TH LETI MEMORY WORKSHOP

Grenoble June 27th





“ If you want to make it faster, you scale it…
if you want to make it more dense, you scale it…
if you want to make it less consuming, you scale it…
if to scale becomes impossible…

you Phase-Change it…”

THANK YOU

ANY Q&A?

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